CALL FOR PAPERS

7th IEEE/ACM International Symposium on Nanoscale Architectures (NANOARCH '11)

Co-located with the 48th Design Automation Conference (DAC)
June 8-9, 2011 San Diego, CA, USA

NANOARCH is the annual cross-disciplinary forum for the discussion of novel post-CMOS nanocomputing directions. The symposium seeks papers on innovative ideas for solutions to the principal challenge facing integrated electronics in the 21st century – how to design, fabricate, and integrate nanosystems to overcome the fundamental limitations of CMOS. In particular, such systems could (1) contain unconventional nanodevices with unique capabilities, including directions beyond simple switches, (2) introduce new logic and memory concepts, (3) involve novel circuit styles, (4) introduce new concepts for computing, (5) reconfigure and/or mask faults at much higher rates than in CMOS, (6) involve new paradigms for manufacturing, and (7) rethink the methodologies and design tools involved.

This 7th symposium introduces, for the first time, several new exciting sessions and opportunities for interaction. In addition to **Regular** papers presenting original techniques/ directions, it invites the community to also submit **Nanofabric Progress Updates** giving a progress update of their nanofabrics directions to date across devices, circuits, architecture and manufacturability aspects – e.g., 2D/3D nanowire, magnonic, memristor, CNT, graphene, FinFETs, and QCA based directions. In addition, **Crosscut** papers are invited from the broader nanotechnology community to highlight promising nanomaterial, nanodevice, nanomanufacturing, and integration ideas with application potential in nanoscale architectures. Example topics (both theoretical and experimental) of interest include (but are not limited to):

- Novel nanodevices and manufacturing/integration ideas with a focus on nanoarchitectures
- Nanoelectronic circuits, nanofabrics, computing paradigms and nanoarchitectures
- 2D/3D/hybrid nanodevice integration and manufacturing, with defect and fault tolerance
- Nanodevice and nanocircuit models, methodologies and computer aided design tools
- Fundamental limits of computing at the nanoscale

Authors are invited to submit papers 4-8 pages in length for the Regular, Nanofabrics Progress Updates and Crosscut Sessions. The electronic submission will be considered evidence that upon acceptance, the author(s) will present their paper at the symposium. Accepted papers will be included in the Symposium Proceedings, published in IEEE Xplore, and considered for the NANOARCH Best Paper Awards. The most exciting papers will be invited to a Special Issue in IEEE Transactions on Nanotechnology.

GENERAL CHAIR: Csaba Andras Moritz, UMass in Amherst (andras@ecs.umass.edu)
PROGRAM CHAIR: Ian O'Connor, Lyon Inst. of Nanotech. (Ian.Oconnor@ec-lyon.fr)
PROGRAM CO-CHAIR: Kang Wang, UCLA (wang@ee.ucla.edu)

Submit papers at http://nanoarch.org by April 10, 2011

Notification of acceptance: May 05, 2011

Early registration deadline: May 09, 2011